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EXAMINER	
RAINEY, ROBERT R	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/583,822	MARX, THILO	
	Examiner	Art Unit	
	ROBERT R. RAINEY	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-20,22-24 and 26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-20,22-24 and 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. The cancellation of claims 21 and 25, which referred to a fourth switching means not shown in the drawings, effectively overcomes the objection to the drawings raised in the previous office action.

2. The amendment to claim 17 such that it now ends with a period effectively overcomes the objection to the claim raised in the previous office action.

3. Applicant's arguments with respect to claim 17-26 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

4. **Claims 17 and 23** objected to because of the following informalities:

Regarding **claim 17**, line 10 of the claim refers to "the first current control" whereas it seems that the proper reference would be to "the first current control **means**" as it was cited in its antecedent reference at line 4.

Regarding **claim 23**, line 14 of the claim refers to "a second current means" whereas it seems that the proper reference would be to "a second current **control** means" in order to be code-congruent with the recitation of "a first current control means" as recited at lines 4-5.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 19 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear what is meant by the substitution required by claim 19. If "a control electrode of a second current control means" is replaced by a "controllable voltage source..." is the controllable voltage source then part of the second current control means and in what manner is it then a current mirror? What does it mean to replace a control electrode with a voltage source? Is a controllable offset voltage to be placed between the control transistor of the current-mirror and the drive transistor of the current-mirror? If the suggested substitute phrase simply replaces the original there are the above problems plus a lack of antecedent basis for "the second current control means" recited in lines 15-16 of the claim.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 17-20, 22-26** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,917,350 to *Pae et al.* ("*Pae*") in view of U.S. Patent No. 7,138,967 to *Kimura* ("*Kimura*").

As to **claim 17**, *Pae* discloses a light emitting display including a multiplicity of elements arranged in rows and columns (see for example Abstract), wherein the elements include a light-emitting means which emits light when a current flows through the light-emitting means (see for example Fig. 2 item "OEL"), a first current control means which is connected in series with the light-emitting means (see for example Fig. 2 item "P0") and, a first (see for example Fig. 3 item 23 "S&H circuit", refer to Fig. 4 to note that item 23 first connects its "ramp" terminal to its "Vramp" terminal and then switches to isolate "ramp" from further changes in "Vramp") and second (see for example Fig. 2 item "P1") switching means which are controlled by a respective first (see for example Fig. 3 the output of comparator 22) and second (see for example Fig. 2 item "SEL") switching signal and which are arranged in the feed to a control electrode of the first current control means (this can be seen by starting at "Vramp" in Fig. 3 and following the signal through the first switch "S&H circuit" to "ramp" through the second switch "P1" to the gate of the first current control means "P0"), wherein a control signal line (see for example Fig. 3 the connection from "Vramp" to "S&H circuit") is connected to one end of the series connection of the first and second switching means (this can be seen by starting at "Vramp" in Fig. 3 and following the signal through the first switch "S&H circuit" to "ramp" through the

second switch "P1" to the gate of the first current control means "P0") of a multiplicity of elements (as noted in the abstract, the disclosure concerns an active matrix device; although the figures and description relate to a single pixel or sub-pixel the figures and description would fairly suggest to one of ordinary skill in the art the repetition of element over rows and/or columns; for example the elements of Fig. 2 repeated for the intersections of all rows and columns resulting in multiple instances of P1 connected to the same data line; duplication at least for every row of at least the elements enclosed by the dashed line in Fig. 3 is implied by the connection of the "ramp" signal to the data line in Fig. 3 and the fact that the circuit doesn't really work for addressing unless the elements of Fig. 3 are duplicated at least for every simultaneously active data line; in describing this case of multiple connections to a single voltage source the specification refers to the signal on the data line as an "externally applied control voltage", see for example 4:27; the same nomenclature is used when describing the relationship of "Vramp" to the "S&H circuit" – see for example 5:3-5, "To the sample & hold circuit 23, an external ramp voltage is applied.", thus implying multiple instances of at least the "S&H circuit" supplied by a common "Vramp";).

Although examiner feels that the above citations show that "Vramp" was taught to connect in parallel to multiple instances of the "S&H circuit", the following is offered since such direct words were not used by *Pae*.

Examiner takes official notice that it was known to those skilled in the art to drive the control terminals of multiple transistors from a single

controlled voltage source. As an example of awareness of this in the prior art, see for example Fig. 4 of the instant application in which transistor 2, responsive to a control signal I_{ref}, generates a controlled voltage that is supplied to three transistors in parallel.

Pae does not provide a drawing showing explicit partitioning and duplication of the elements of Fig. 3 and in particular does not show a drawing of a single "Vramp" signal connected to multiple "S&H circuit"s. The limits of the partitioning, however, are easily determined: at one extreme duplicating a given element once for the display and at the other extreme duplicating that element for every pixel. Given *Pae*'s notice that the "Vramp" signal was supplied from a circuit "external" to that shown in Fig. 3 and the knowledge that a voltage signal can be used to drive the gates of multiple transistors, the limits concerning the generators for "Vramp" are from one per display to one per "S&H circuit". At the time of the invention it would have been obvious to one of ordinary skill in the art to arrive at an implementation of *Pea* including the connection of a multiplicity of "S&H circuit"s, i.e. first switches to each "Vramp", i.e. controllable voltage source.

Thus *Pae* discloses or reasonably suggests to one of ordinary skill in the art the claimed invention except for the first switch being provided in each element and the use of a controllable voltage source in which a control electrode of a second current control means is connected to the control signal line such

that the multiplicity of the first current control means and the second current control means form a correspond multiplicity of current mirror circuits connected in parallel when the respective first and second switching means are conducting.

Kimura discloses (Here examiner repeats citations for elements already taught in *Pea* in order to point out the fundamental similarity between the circuits disclosed in *Kimura* and *Pea*. For ease of reference, citations for the elements not taught in Pea are set off by a paragraph break below.) a display device and driving method for a multiplicity of elements arranged in rows and columns comprising a first switching means (see for example Fig. 44 item 1448) provided in each element which is controlled by a first switching signal (see for example Fig. 44 "dot-sequential line CLP"), and a second switching means (see for example Fig. 44 item 1444) which is arranged in series with the first switching means in the feed to the control electrode of a first current control means (see for example Fig. 44 item 112 "current supply transistor") and which is controlled by a second switching signal (see for example Fig. 44 "signal line GH") to store a current control voltage (see for example Fig. 44 "Vgs" of item 1445) that is generated by means of

a controllable voltage source comprising a second current control means (see for example Fig. 44 transistor 1445) in which a control electrode of the second current control means (see for example Fig. 44 transistor 1445) is connected to a control signal line (see for example Fig. 44 the line connecting to transistor 1448 to which the line connecting to the gate of transistor 1445

connects) such that the first current control means and the second current control means form a corresponding current mirror circuit when the respective first and second switching means are conducting (see for example Fig. 44, note that current transistor 1445 is responsive to a control current supplied through current line CL and forms a current mirror circuit with current supply transistor 112).

Pae and *Kimura* are analogous art because they are from the same field of endeavor, which is active matrix displays.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to improve the circuit of *Pae* by using a controllable voltage source comprising a transistor connected in a current-mirror configuration as taught by *Kimura* as the controllable voltage source of *Pae*. The suggestion/motivation would have been to provide advantages such as to ensure that a constant current flows irrespective of fluctuation in threshold voltage, mobility, or the like (see for example Kimura 5:38-45) or to use an art recognized type of controllable voltage source or to use a type of controllable voltage source that inherently compensates for some noise and degradation factors (see for example *Kimura* 8:52-54 "same current characteristics").

At the time of invention, it would have been obvious to a person of ordinary skill in the art to improve the circuit of *Pae* by repeating the "S&H circuit" function of Pae in each element as taught by *Kimura*. The suggestion/motivation would have been to provide advantages such as to allow the current level to be

set in a dot-sequential fashion (see for example 59:9-17) or to use a known alternative addressing circuit.

As to **claim 18**, in addition to the rejection of claim 17 over *Pae* and *Kimura*:

Pae further discloses a drive voltage signal cyclically falling from a predetermined starting value to an end value applied to a terminal of the switching means (see for example Fig. 2-4 "ramp").

Kimura further discloses the controllable voltage source controlled by a drive signal (see for example Fig. 44 "current line CL") switchably supplied to the second current control means via third switching means (see for example Fig. 44 item 1443), wherein the control signal supplied to the control electrode of the first current control means is dependent on the drive signal (see for example Fig. 44).

Pae and *Kimura* disclose the claimed invention except for the signal rising instead of falling. Since both rising and falling ramps were known to those skilled in the art and positive and negative voltage driven transistors were known it would have been obvious to one skilled in the art to replace a positive going ramp for a negative going ramp. One of ordinary skill could have implemented the modification and it would not have been beyond the reach of ordinary skill to consider both alternatives.

As to **claim 19**, in addition to the rejection of claim 17 over *Pae* and *Kimura*:

Already disclosed in the rejection of claim 17 is the teaching that current control means is a controllable voltage source applied from the control electrode.

As to **claim 20**, in addition to the rejection of claim 17 over *Pae* and *Kimura*, both *Pae* and *Kimura* further disclose a signal holding means connected to the control electrode of the first current control means wherein the control signal is held when the first and/or second switching means interrupts the supply of the control signal to the control electrode of the first current control means (see for example the capacitors of Pae Fig. 2 "Cs" and Kimura Fig. 44 item 111).

As to **claim 22**, in addition to the rejection of claim 17 over *Pae* and *Kimura*, *Kimura* further discloses a common first switching signal is supplied to a plurality of first switching means in elements in a line and/or a column (see for example Fig. 45).

Claim 23 claims the method implicit in the rejection of claim 18 plus the rejection of claim 17 and is rejected on the same grounds and arguments.

Claim 24 claims the method implicit in the rejection of claim 22 plus the rejection of claim 18 plus the rejection of claim 17 and is rejected on the same grounds and arguments.

As to **claim 26**, in addition to the rejection of claim 23 over *Pae* and *Kimura*, *Pae* further discloses an idle time provided between two cycles (see for example Fig. 4 period T2, which shows a flat or idle period in Vramp between the ramping cycles).

Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT R. RAINEY whose telephone number is (571)270-3313. The examiner can normally be reached on Monday through Friday 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on (571) 272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/RR/

/Amare Mengistu/

Supervisory Patent Examiner, Art Unit 2629